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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,970	04/06/2001	Alasdair Rawsthorne	1801270.00122US1	5419

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/29/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/29/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	09/827,970	RAWSTHORNE ET AL.	
	Examiner	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' argument on 10/16/2006 ("Pre-Appeal Conference"). The finality is withdrawn. Following is a new ground of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al, US patent no. 6,199,152 B1 in view of Gamo, Tsutomu, US patent no. 6,279,121 B1.

As per claim 1, Kelly discloses a method and system for processing and protecting memory for a computer processor during normal and emulation operation with feature limitations very similar to the claimed invention. According to Kelly, the memory processing method includes steps

Mapping target register representing a working register of a subject machine for exception emulation to move data to either a first location or to a second location within a target machine (Fig. 4, "Register File", col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register subject to exception handling between the first and second locations, registers required space in memory for storing data, for code

translation/conversion for exception emulation. Kelly does not expressly disclose mappings registers in alternative manner as object abstract as claimed. Such claimed feature is however well-known in the art. In fact, Gamo teaches a plural of abstract registers for mapping and handling exceptions simultaneously in a plural exception processing (col. 2, lines 57-67, col. 13, lines 34-60). Such object registers are called abstract registers in object processing (col. 13, lines 34-43, cols. 14-17).

This would motivate practitioner in the art at the time of the invention was made to combine Gamo teaching of exception handling in object registers and processing or mapping the object registers in each application and event into Kelly to simultaneously handling a plural of exceptions.

As per claim 2, Gamo discloses instruction codes objects, location space to hold a content or a definitive value of the abstract register, while the other of locations holds a speculative for handling exception during code conversion or emulation as claimed.

As per claim 3, Kelly discloses code conversion and code optimization including the limitations as claimed for target emulation.

As per claim 4, Kelly discloses register mapping for predetermined section of subject code as claimed (col. 13, lines 39-61, col. 16, lines 20-40, for example).

As per claim 5, Gamo teaches a plurality of abstract or object registers for selected target locations as above for handling exception as event object (Fig. 7, 8, cols. 14-15).

As per claims 6-8, Kelly discloses the claimed limitation during code translation for handling code exception.

As per claim 9, Kelly discloses a method for use in handling exceptions by an emulator performing program code conversion between subject code suitable for a first type (subject) processor and target code suitable for a target processor with feature limitations very similar to the claimed invention. According to Kelly, the method for code conversion in the target emulation includes steps:

Providing a plurality of registers of the first type processor (Fig. 4),

Mapping the target register representing a working register of a subject machine for emulation to either a first location or to a second location within a target machine (col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register subject to exception handling between the first and second locations for code translation/conversion for exception emulation. Kelly does not expressly disclose mappings registers in alternative manner as object abstract as claimed. Such claimed feature is however well-known in the art. In fact, Gamo teaches a plural of abstract registers for mapping and handling exceptions simultaneously in a plural exception processing (col. 2, lines 57-67, col. 13, lines 34-60). Such registers are called object or abstract registers in object processing (col. 13, lines 34-43, cols. 14-17).

This would motivate practitioner in the art at the time of the invention was made to combine Gamo teaching of exception handling in object registers and processing or

mapping the object registers in each application and event into Kelly to simultaneously handling a plural of exceptions.

As per claim 10, Kelly discloses for a predetermined section or set of instruction codes, locations holding a content or a definitive value of the abstract register, while the other of locations holds a speculative for handling exception during code conversion or emulation, and the mapping is performed upon reaching the end of the predetermined subject code as claimed.

As per claim 11, Kelly and Gamo disclose a code conversion including the limitations as claimed for target emulation.

As per claims 12-13 and 14-15, due to the similarity of claims 12-13 and 14-15 to the rejected claims above, and Kelly discloses an emulator and computer program product for use in handling exceptions by an emulator performing program code conversion between subject code suitable for a first type (subject) processor and target code suitable for a target processor with feature limitations very similar to the claimed invention. According to Kelly, the emulator with program product includes means for performing steps

Providing a plurality of registers of the first type processor (Fig. 4),

Mapping target register representing a working register of a subject machine for emulation to either a first location or to a second location within a target machine (col. 15, lines 26-46, col. 16, lines 20-40, col. 23, line 1-11, col. 32, lines 40-64, for example),

Mapping of the working register subject to exception handling between the first and second locations for code translation/conversion for exception emulation. Kelly

does not expressly disclose mappings registers in alternative manner as object abstract as claimed. Such claimed feature is however well-known in the art. In fact, Gamo teaches a plurality of abstract registers for mapping and handling exceptions simultaneously in a plural exception processing (col. 2, lines 57-67, col. 13, lines 34-60). Such registers are called object or abstract registers in object processing (col. 13, lines 34-43, cols. 14-17).

This would motivate practitioner in the art at the time of the invention was made to combine Gamo teaching of exception handling in object registers and processing or mapping the object registers in each application and event into Kelly to simultaneously handling a plural of exceptions.

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,560,013, issued to Scalzi et al, on Sept. 1996
2. US patent no. 5,933,642, issued to Greenbaum et al, on Aug. 1999
3. US patent no. 6,260,190 B1, issued to Ju, Dz-Ching, on July 2001

4. US patent application publication no. 2002/0046305 A1, issued to Babaian et al, Apr. 2002

5. US patent no. 6,075,942, issued to Cartwright, Robert, on June 2000

6. US patent application publication no. 2002/011227 A1, issued to Kramskoy et al, on Aug. 2002

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

3. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jan. 19, 2007

Thai Phan

THAI PHAN
PRIMARY EXAMINER
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